

FIG. 2 (PRIOR ART)

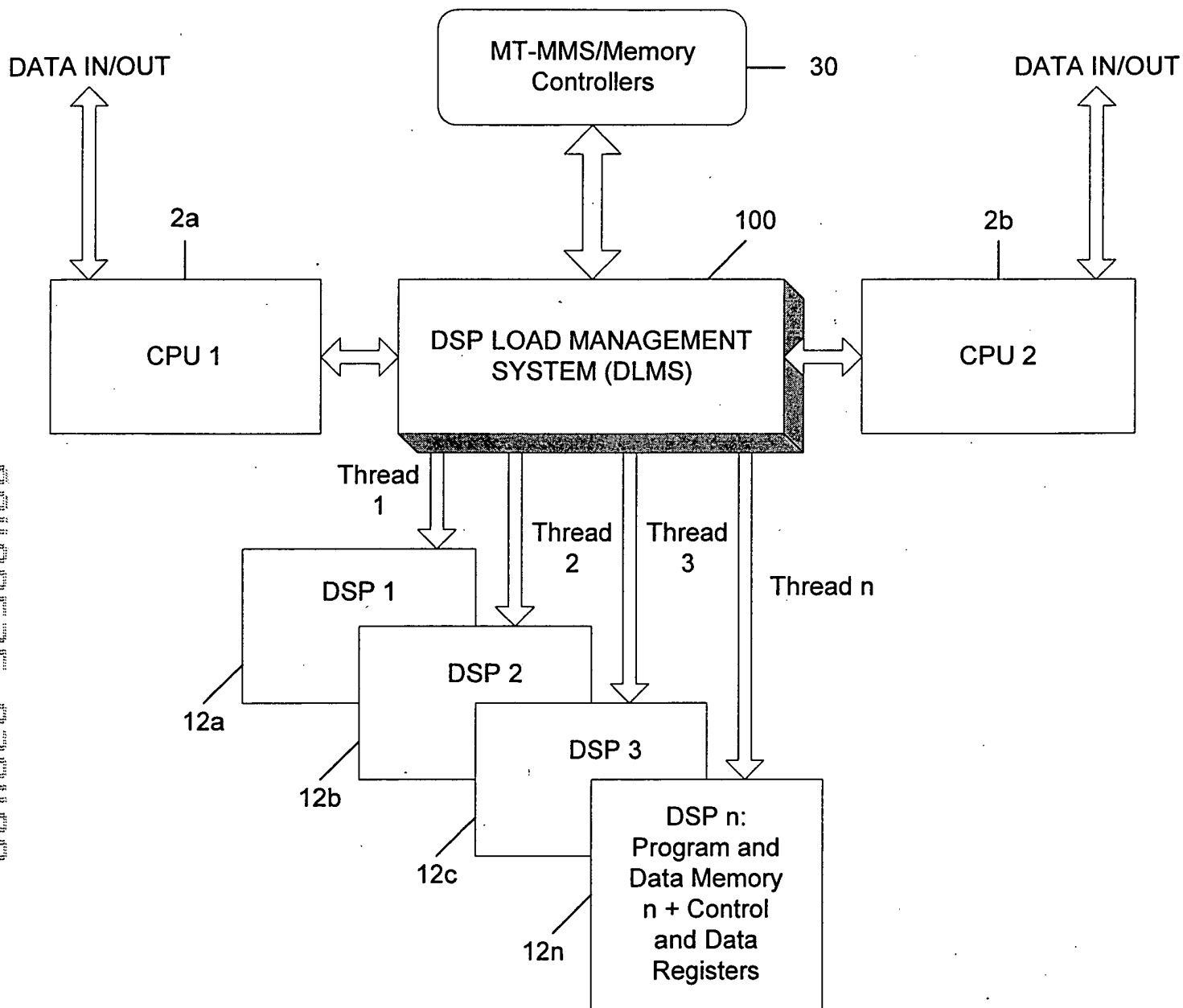


FIG. 3A

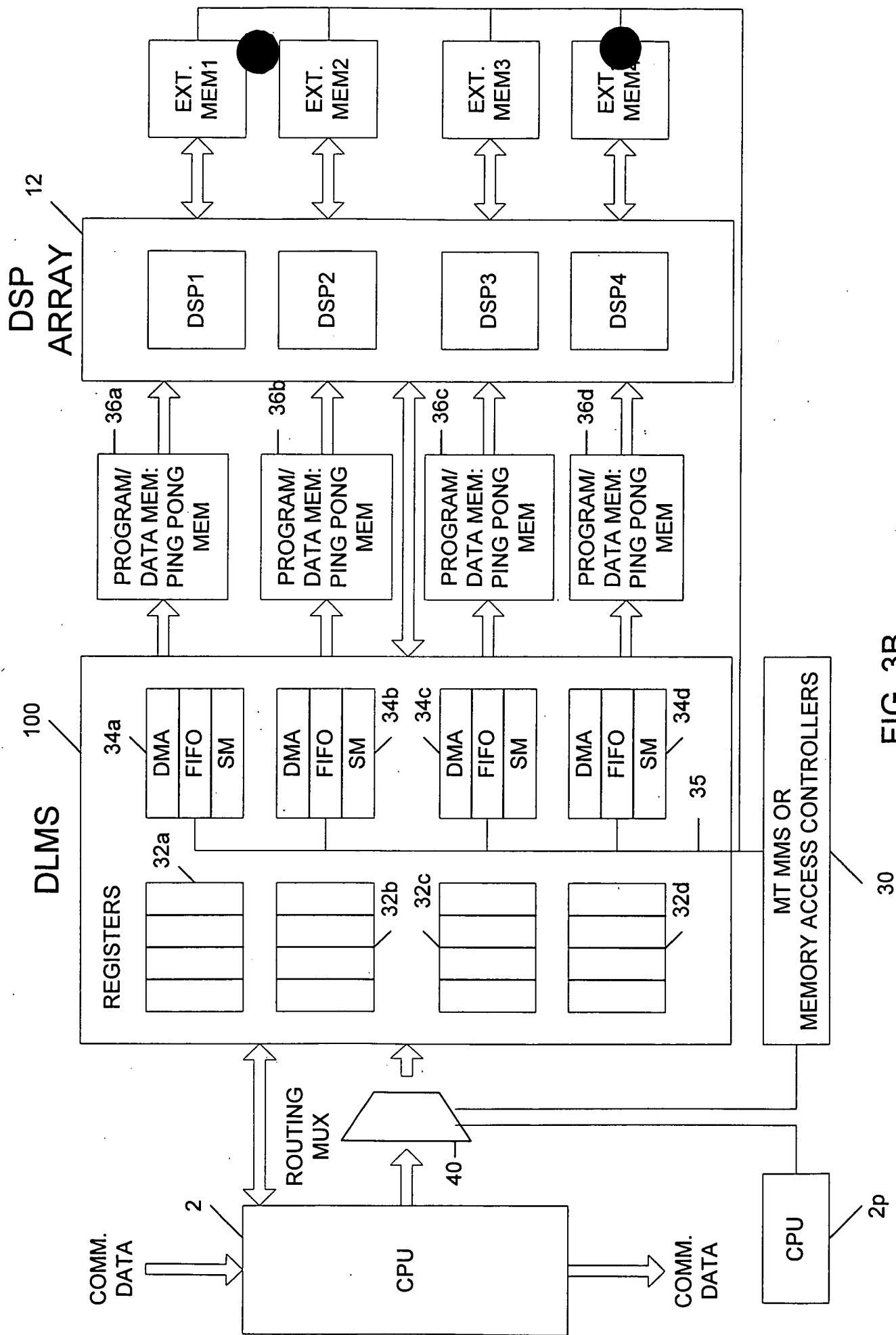
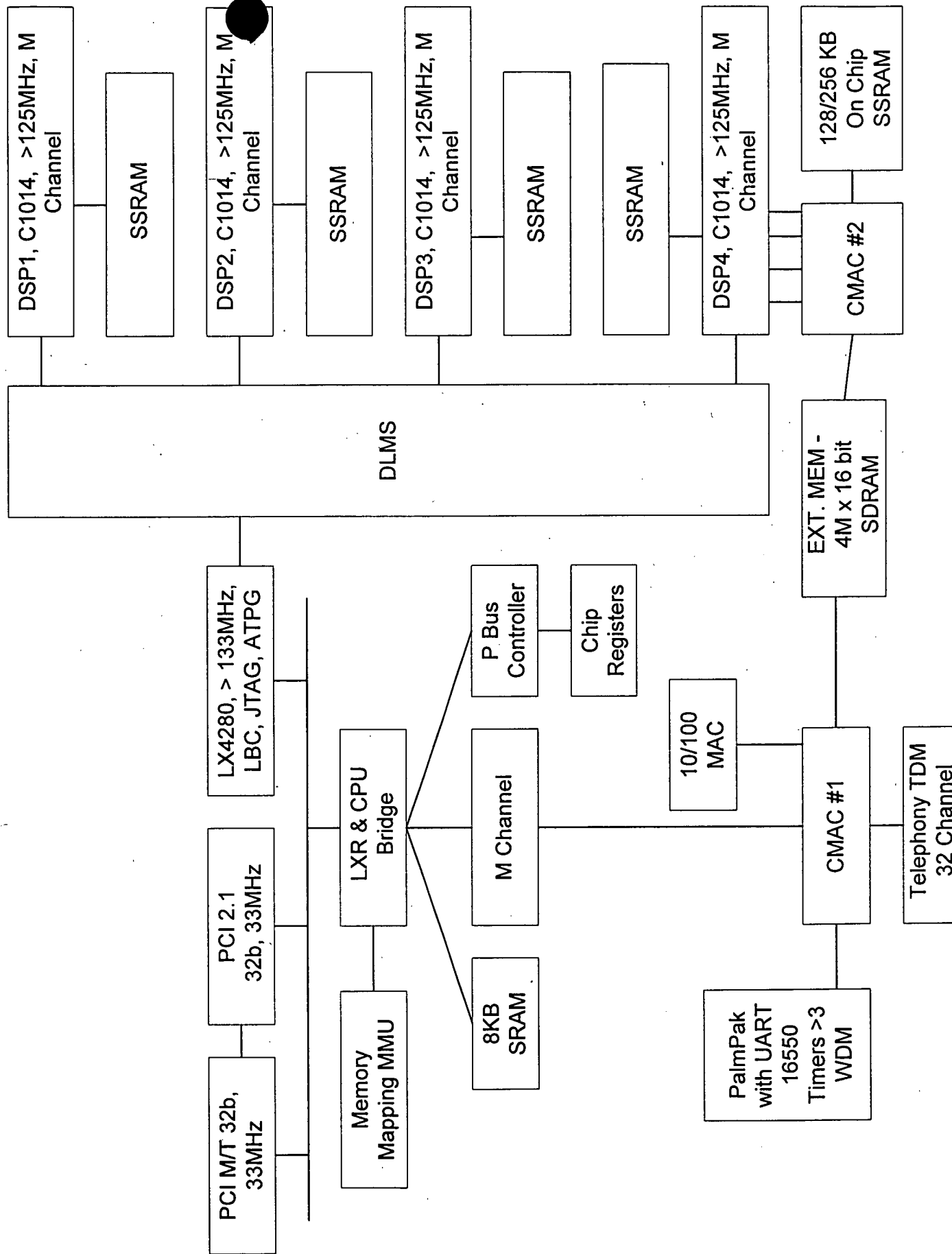


FIG. 3B

FIG. 3C



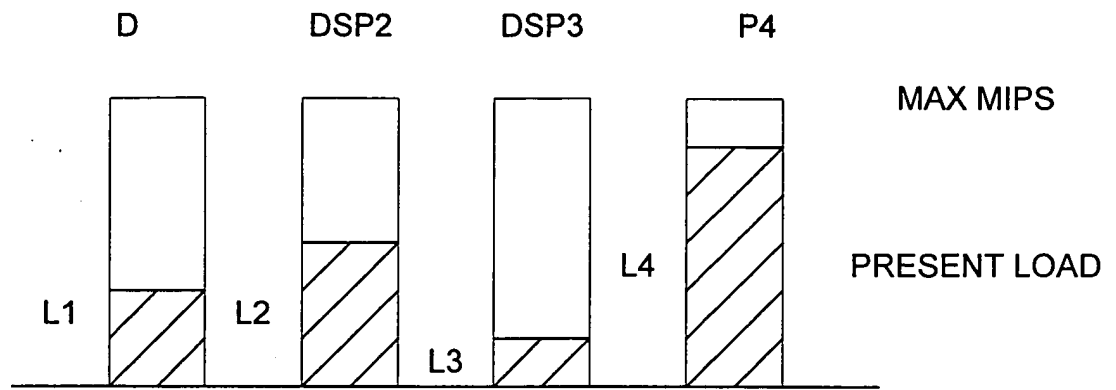


FIG. 4A

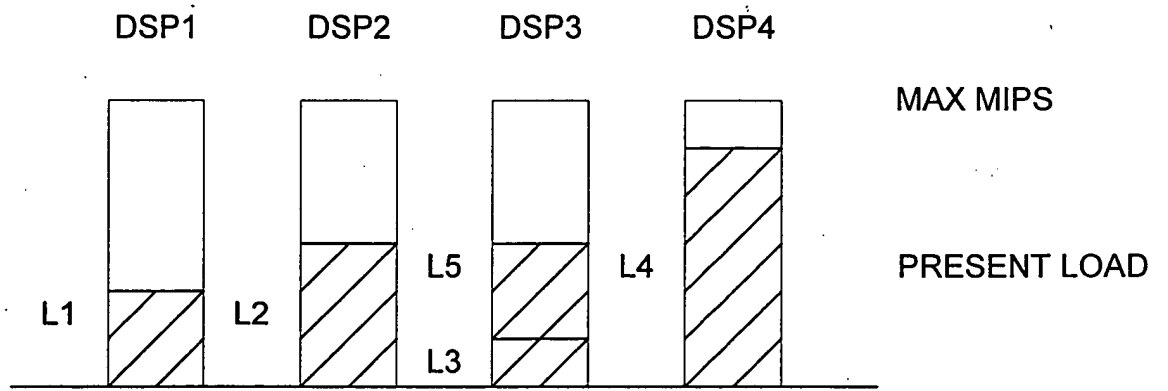


FIG. 4B

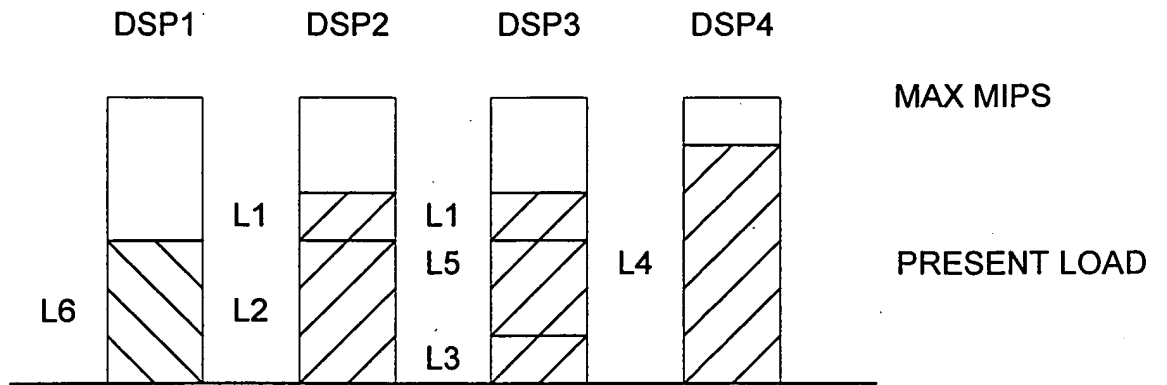


FIG. 4C

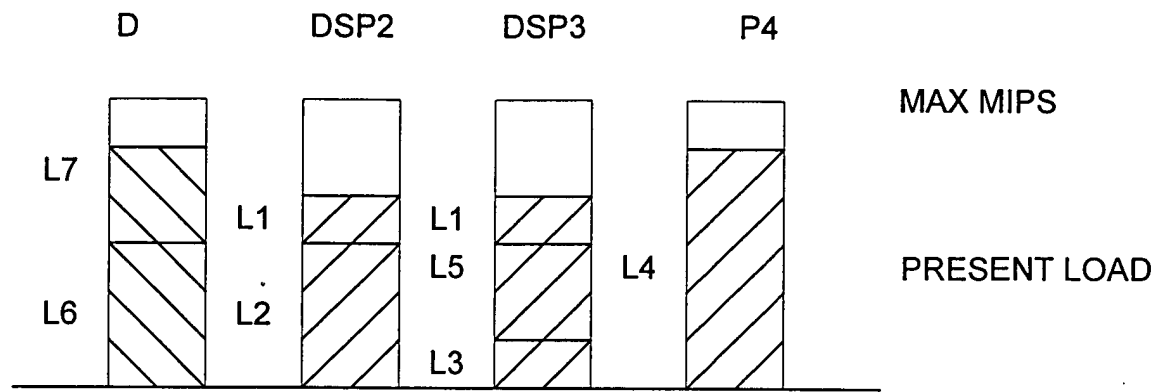


FIG. 4D

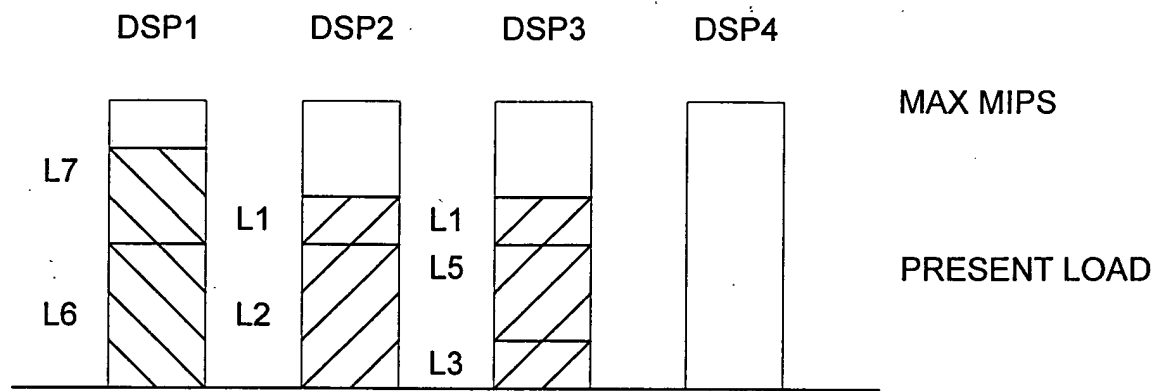


FIG. 4E

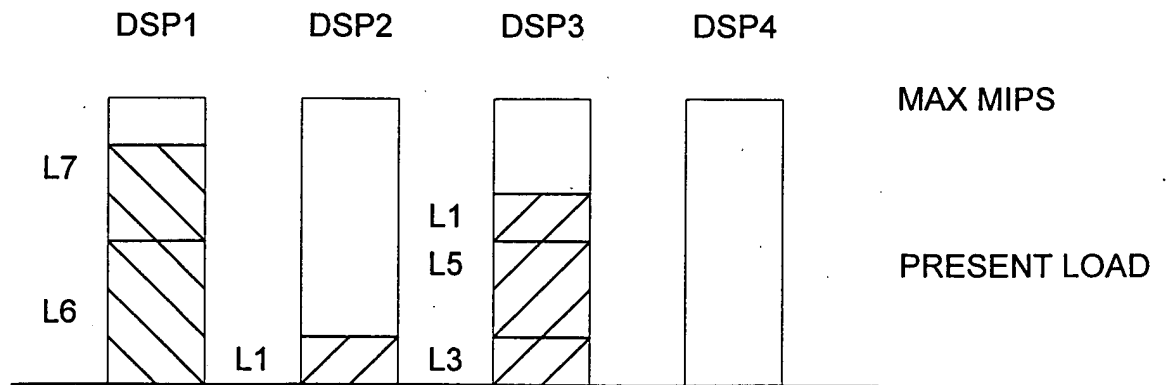


FIG. 4F

| | DSP1 | DSP2 | DSP3 | |
|-------------|------|------|------|--|
| ALGORITHM 1 | 15 | | | |
| ALGORITHM 2 | | 5 | | |
| ALGORITHM 3 | | | 2 | |
| ALGORITHM 4 | | | 2 | |

FIG. 4G

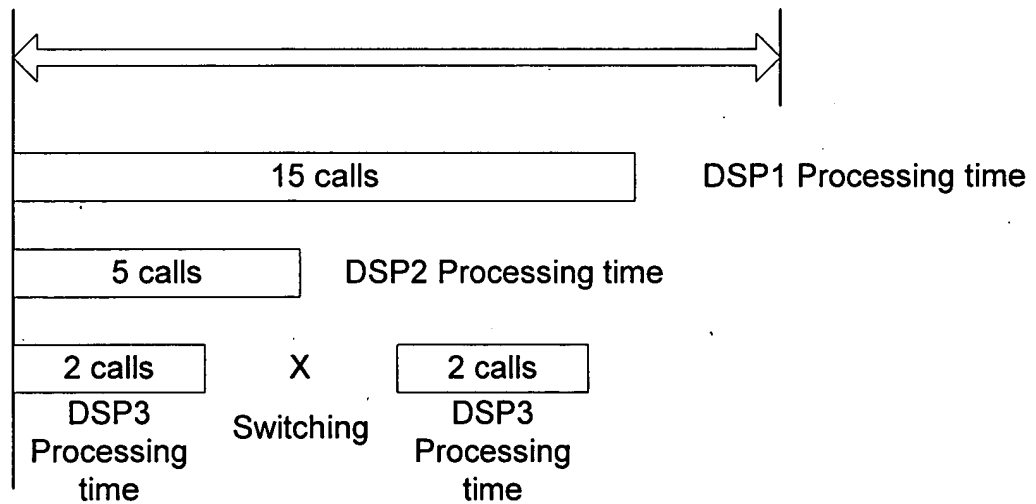


FIG. 4H

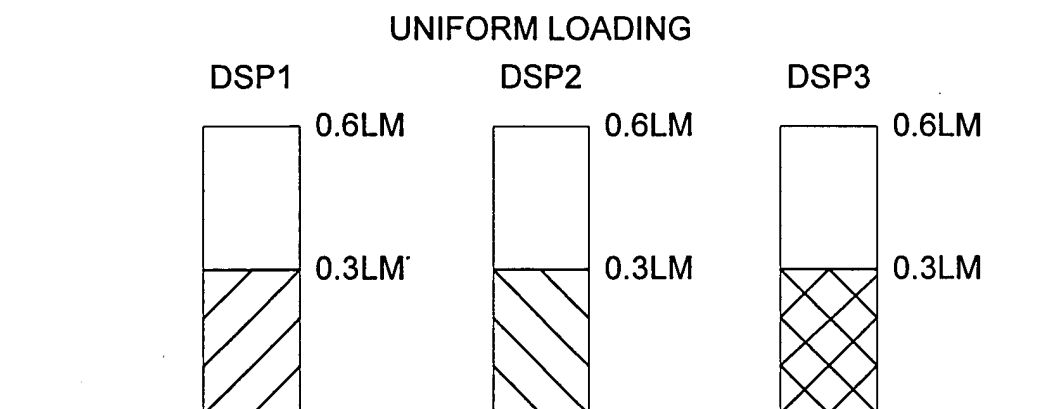


FIG. 5A

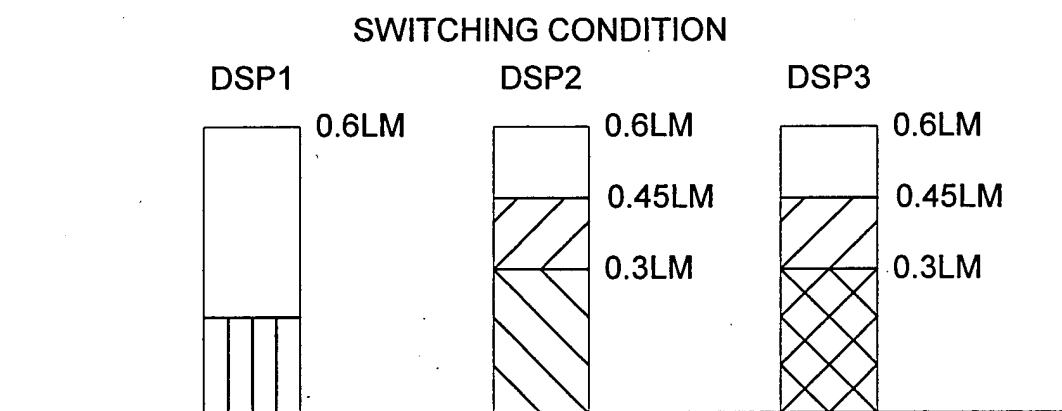


FIG. 5B

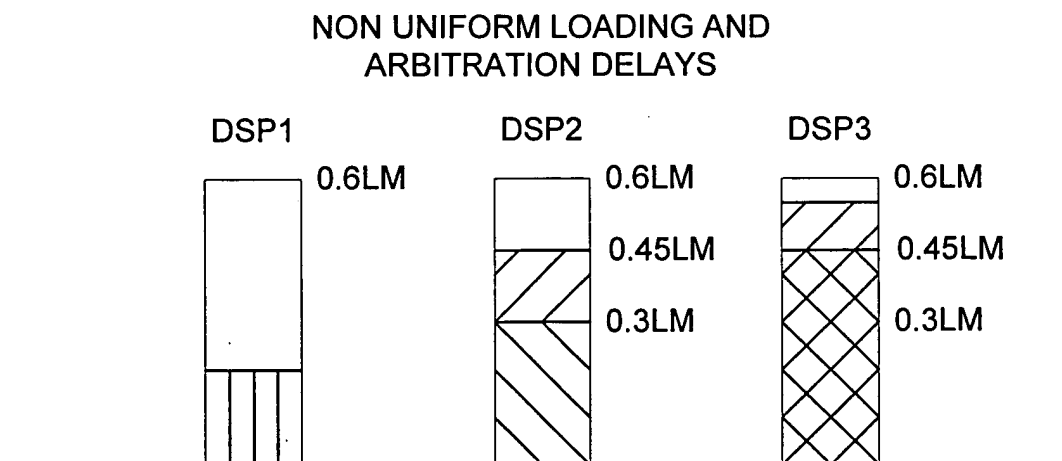


FIG. 5C

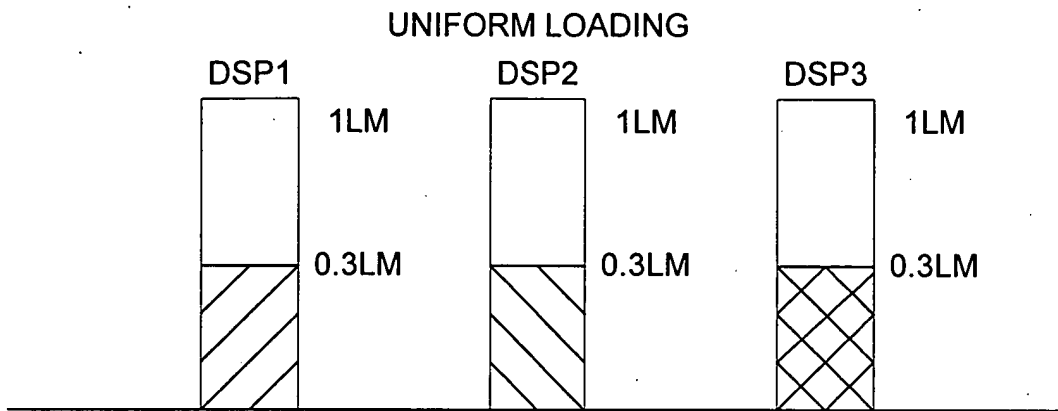


FIG. 6A

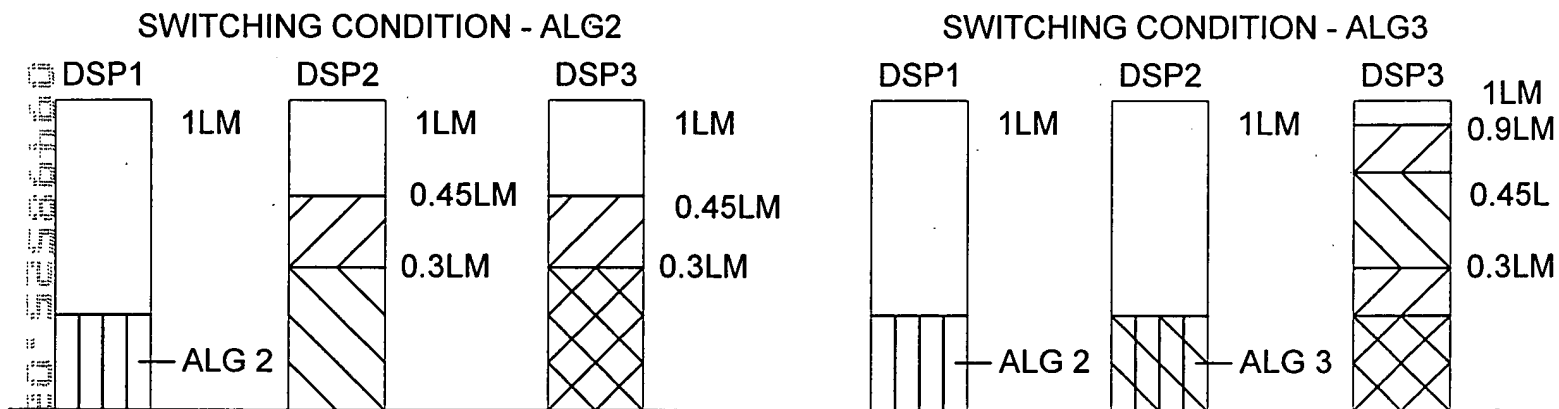


FIG. 6Bi

FIG. 6Bii

NON UNIFORM LOADING AND
ARBITRATION DELAYS

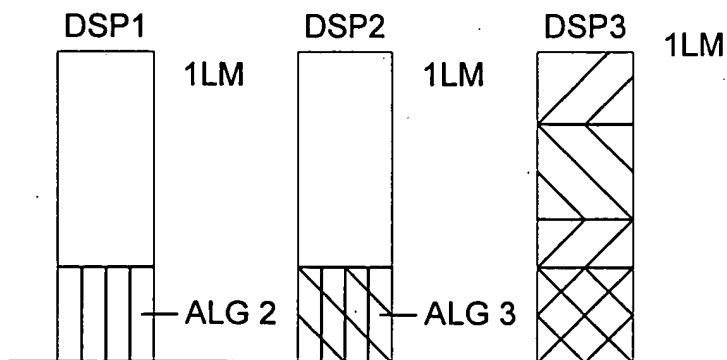
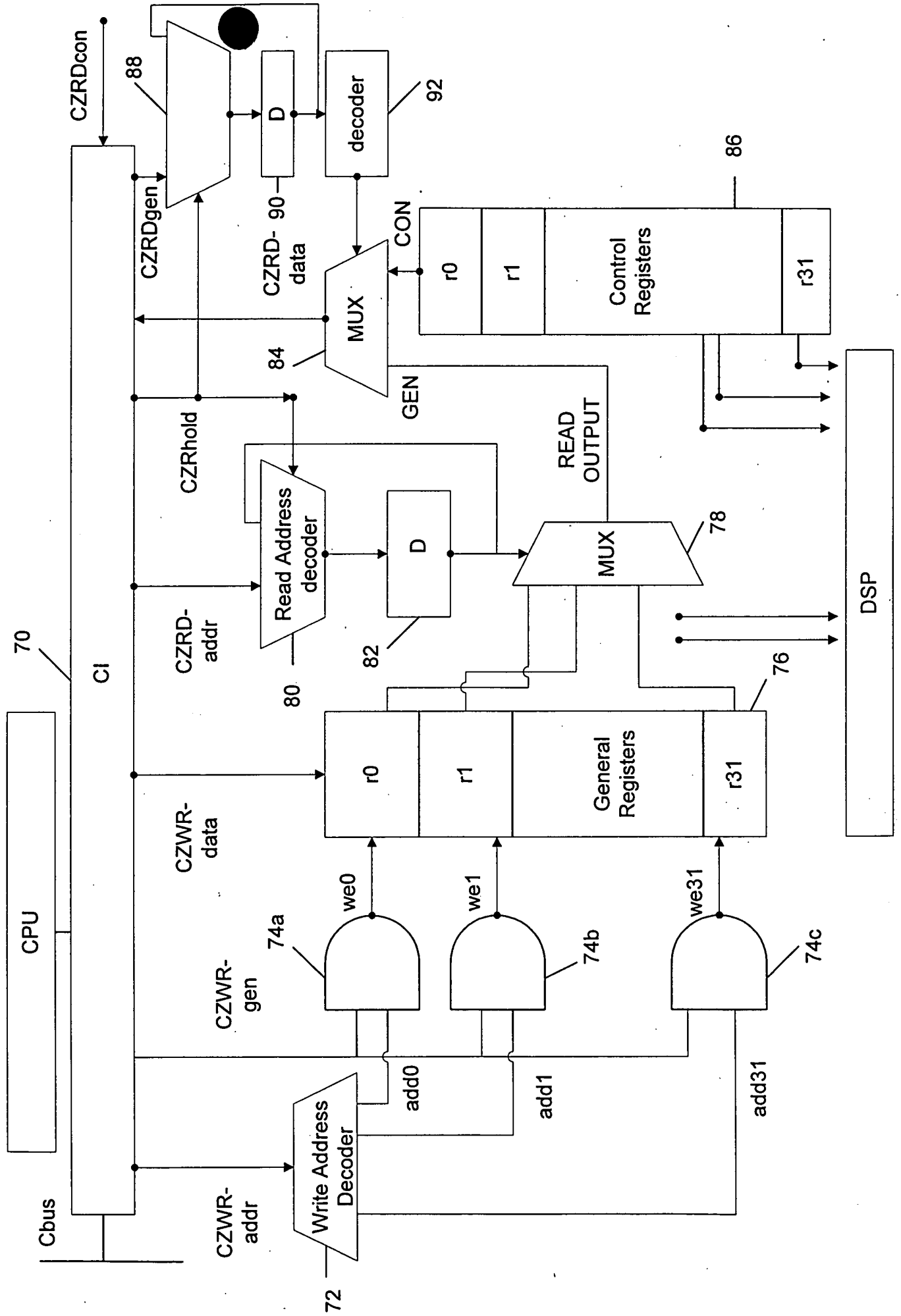


FIG. 6C

FIG. 7A



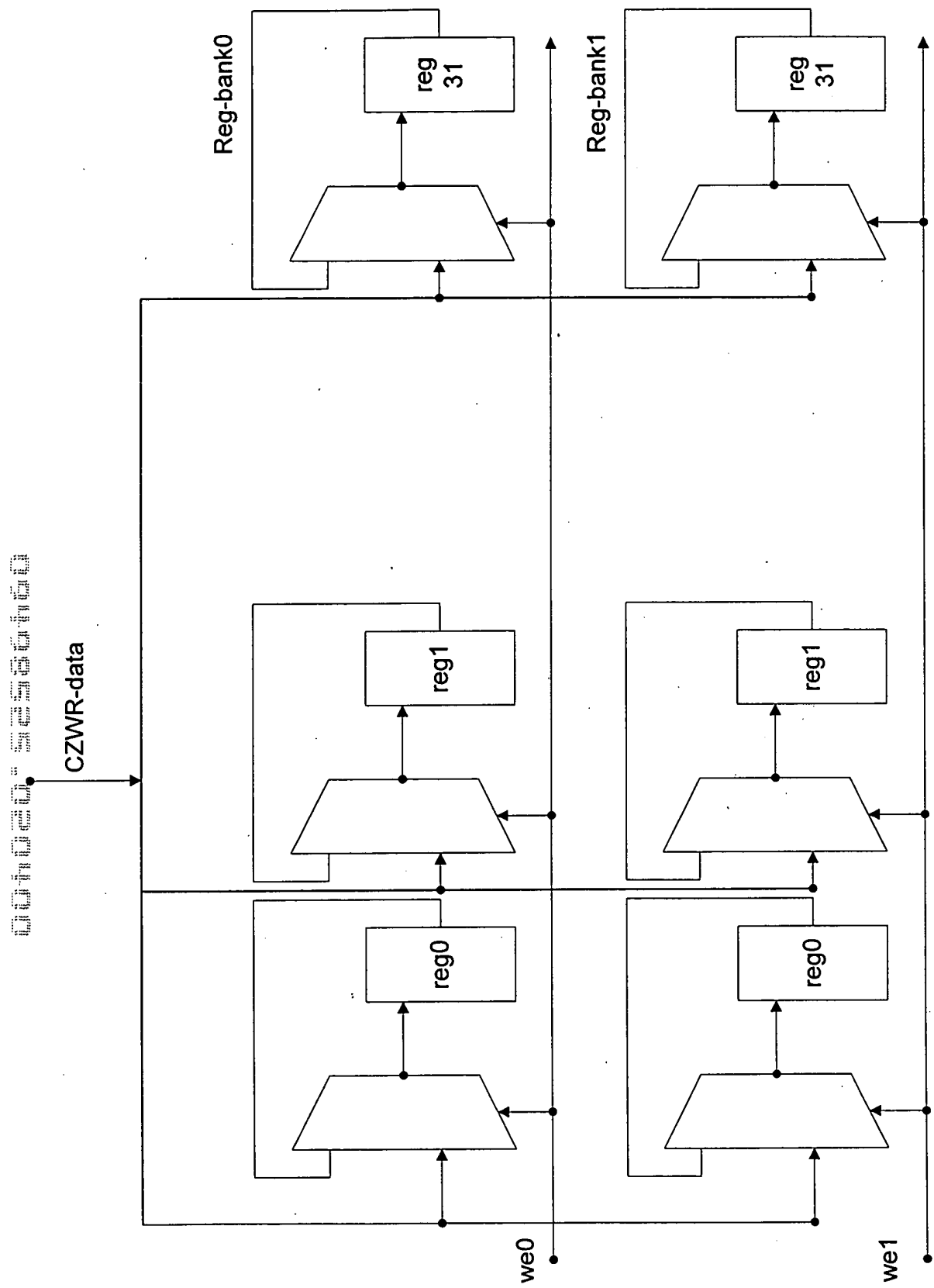


FIG. 7B

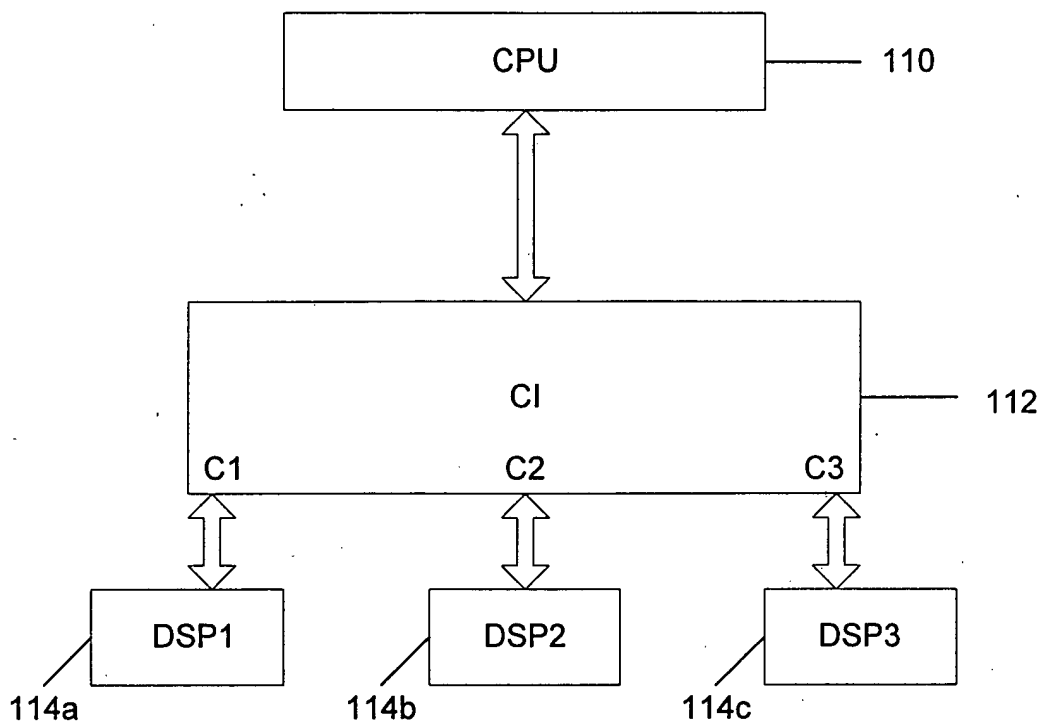


FIG. 8A

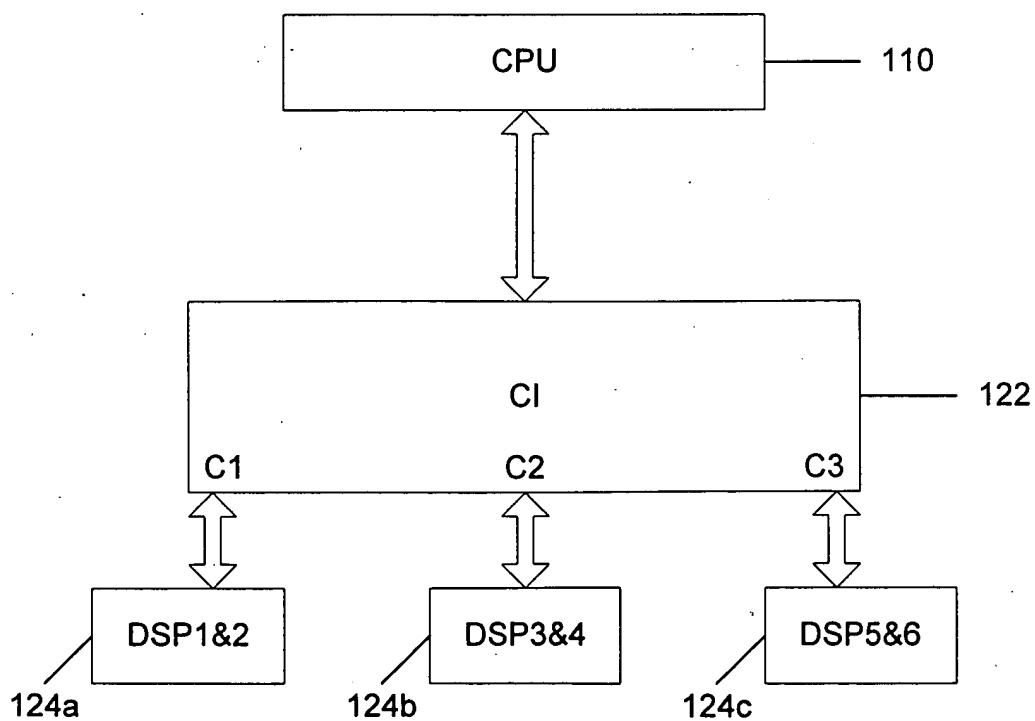


FIG. 8B

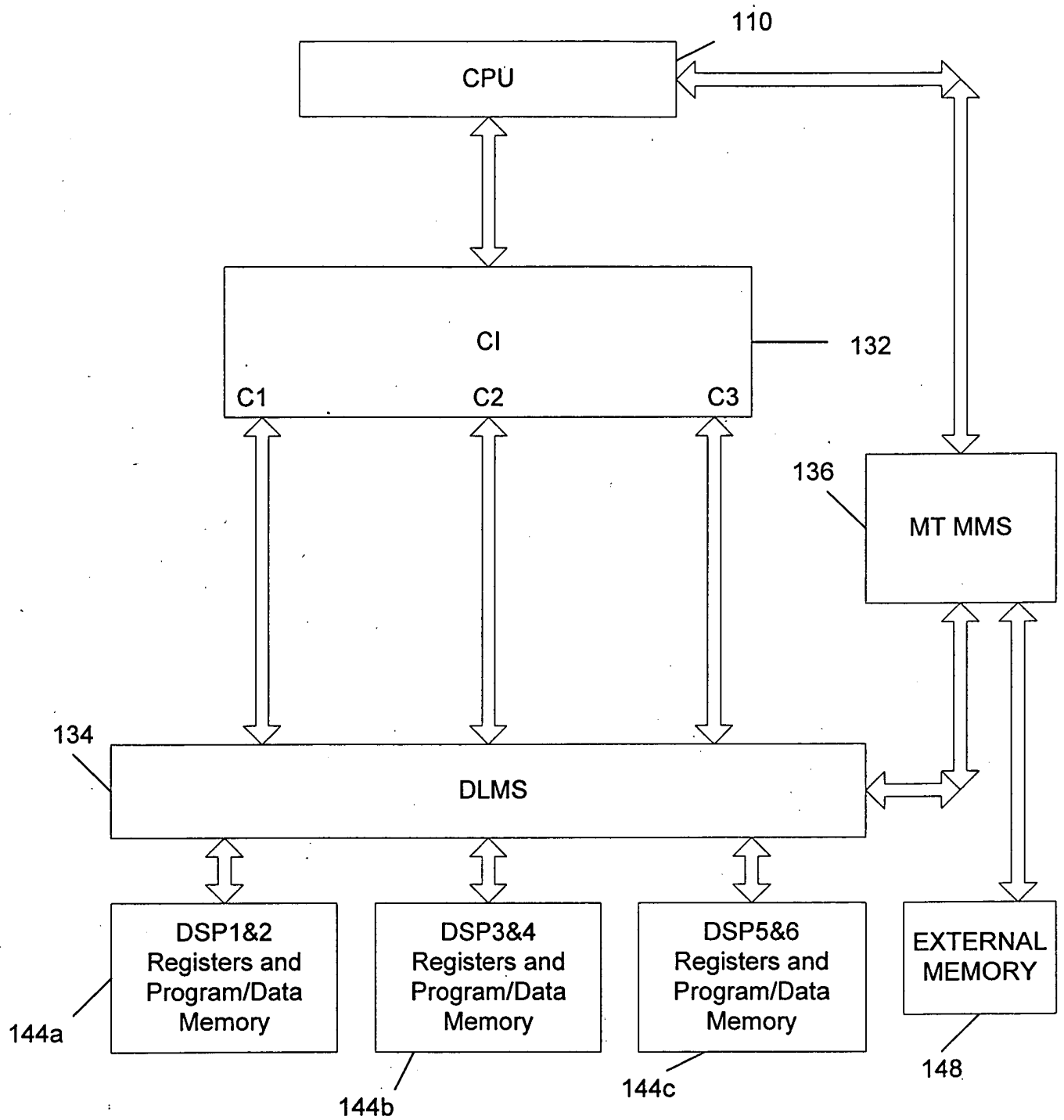


FIG. 9A

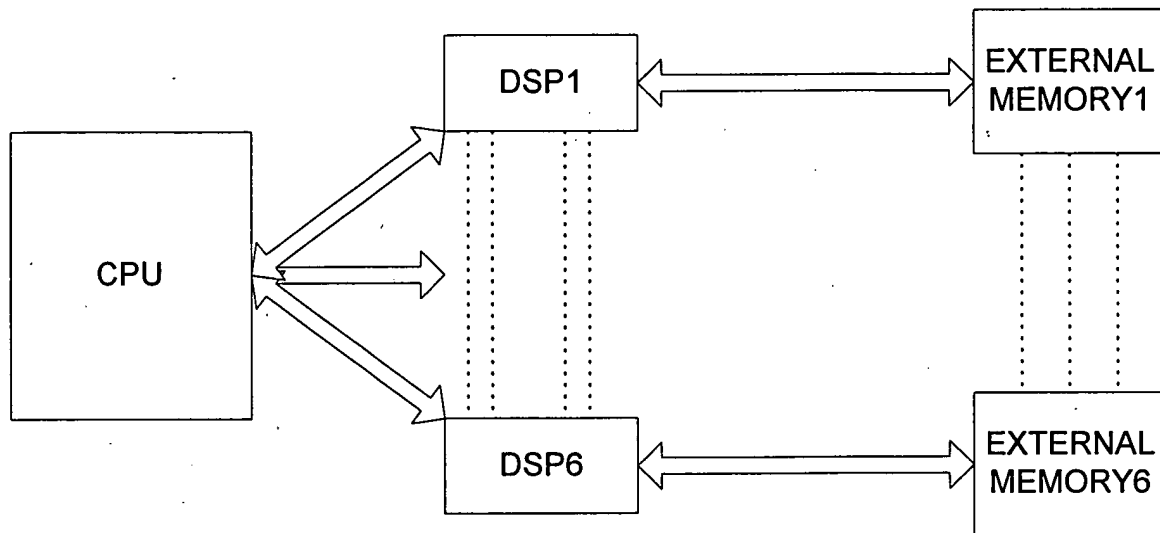


FIG. 9B

MT MMS LOADING DSP WITH HF DATA

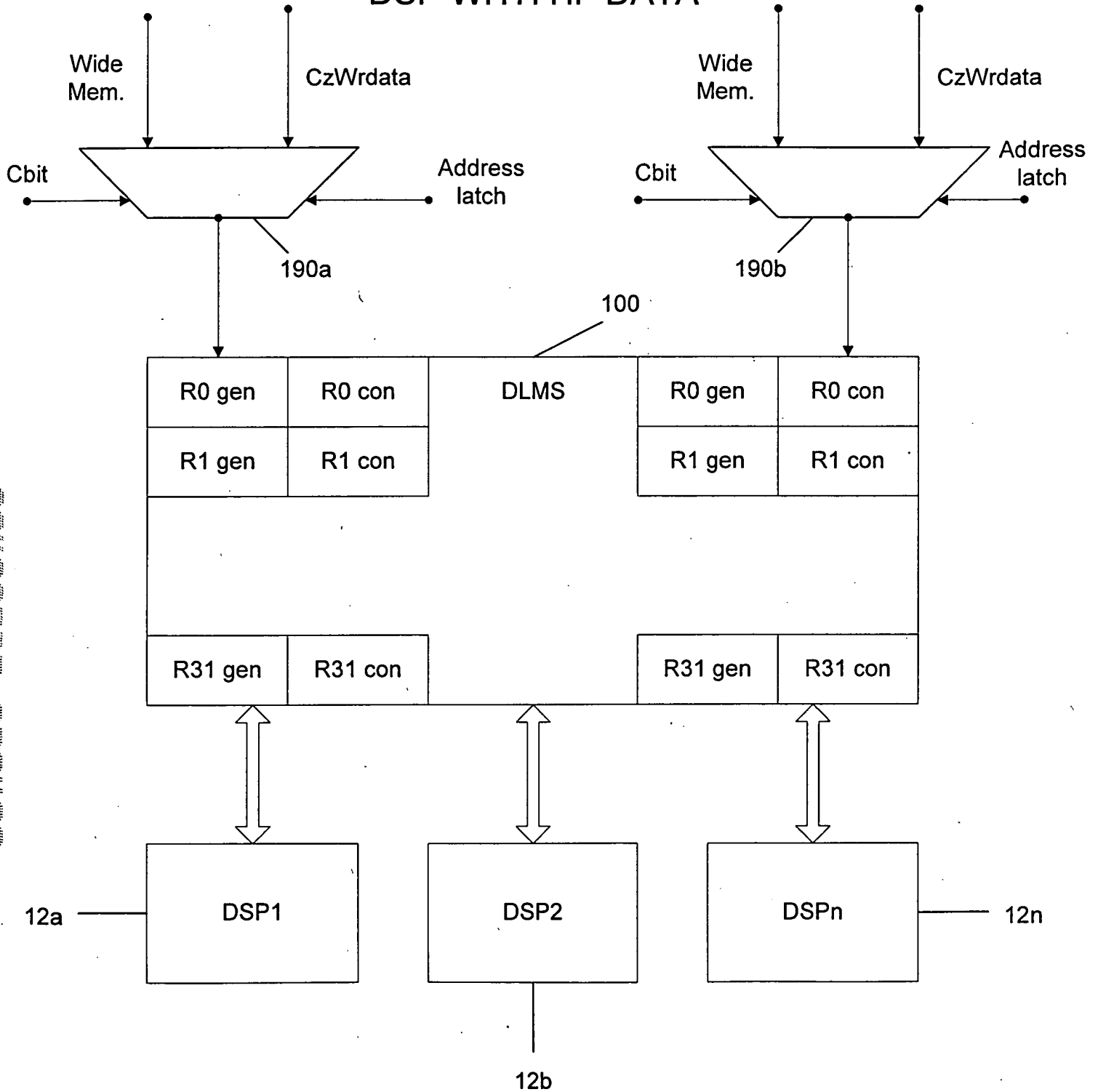


FIG. 10

2 MAC CLUSTER

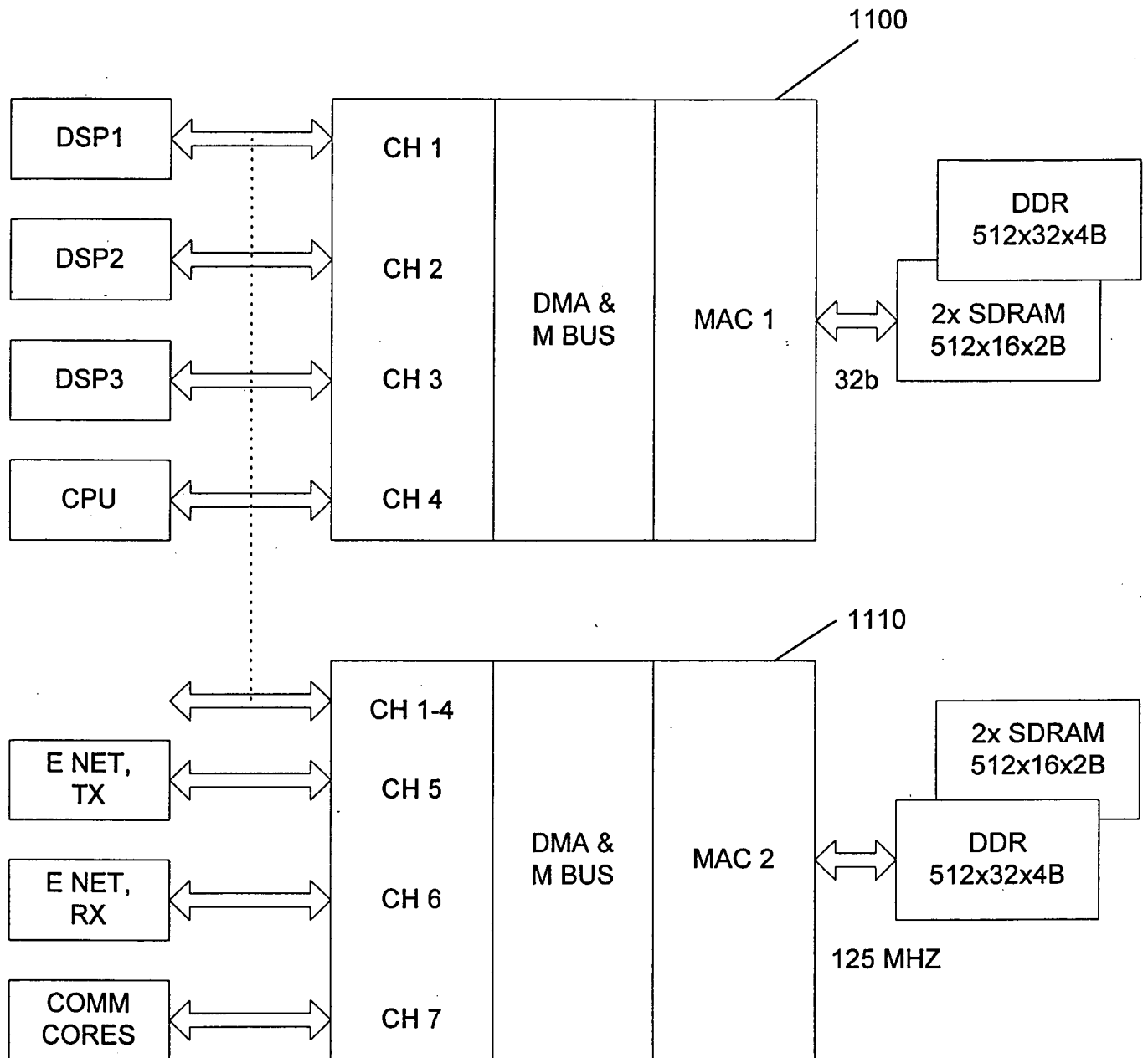


FIG. 11

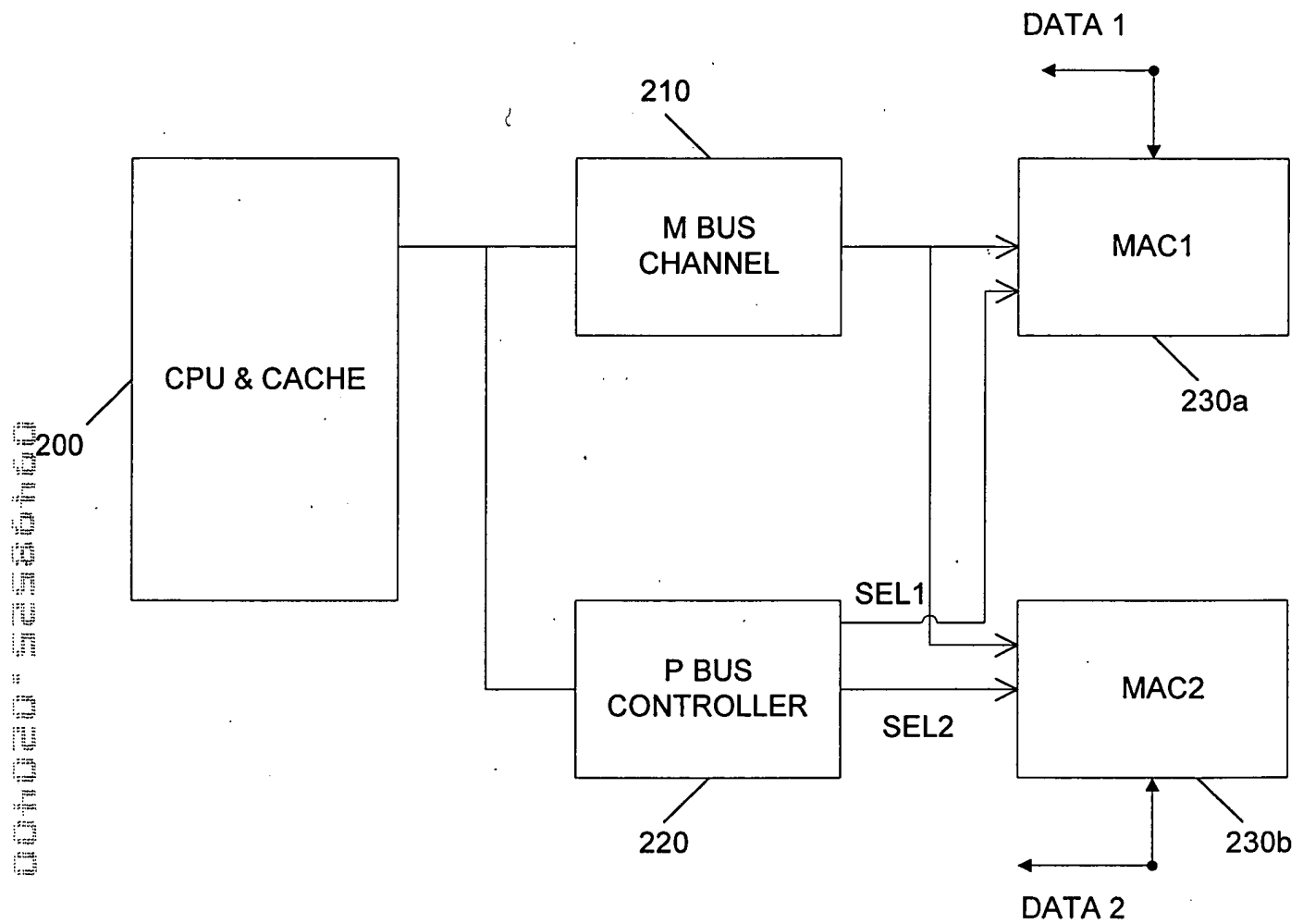


FIG. 12

DMA & MAC CLUSTER

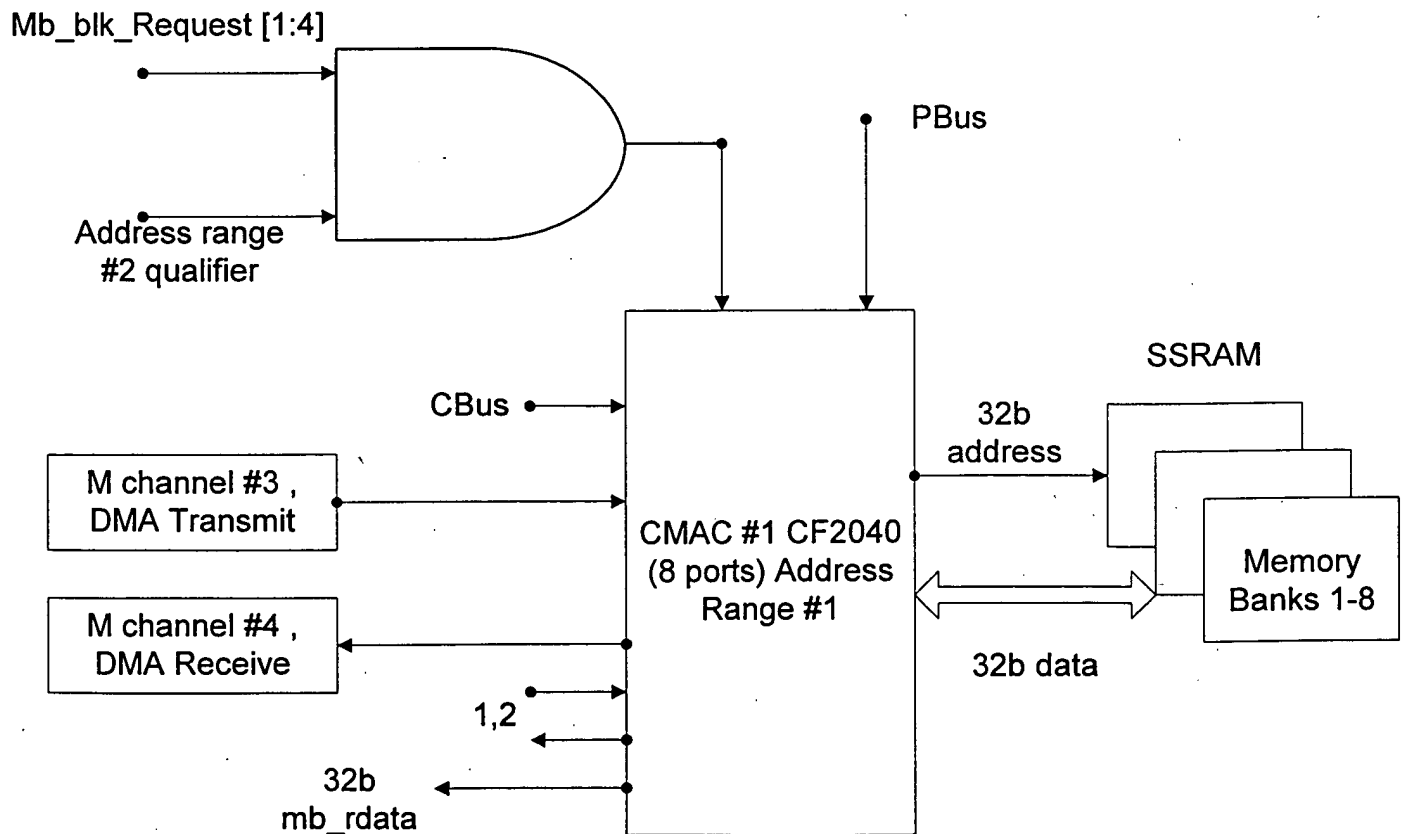
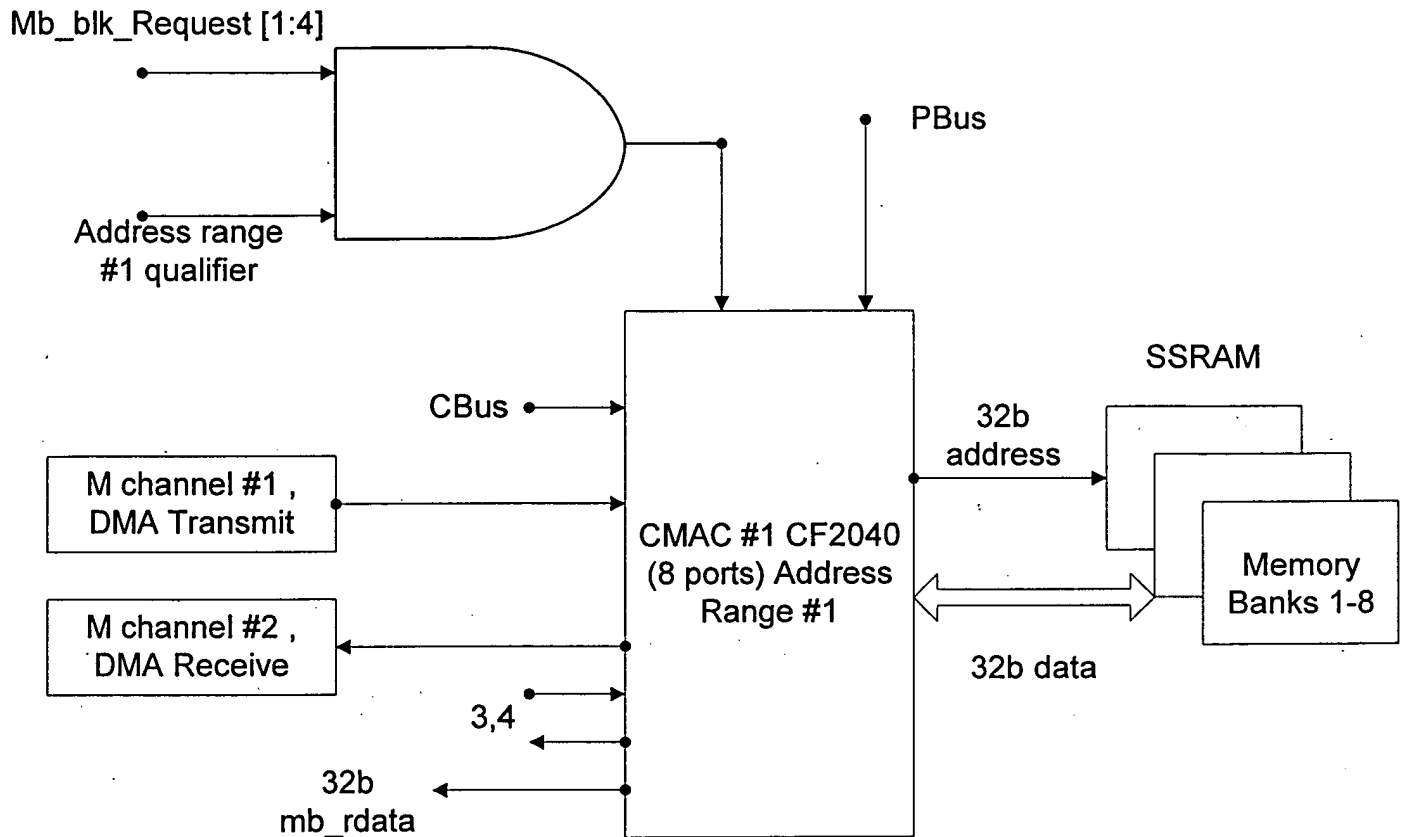


FIG. 13

MULTIPLEXING THE DATA BUS TO INDIVIDUAL CHANNELS

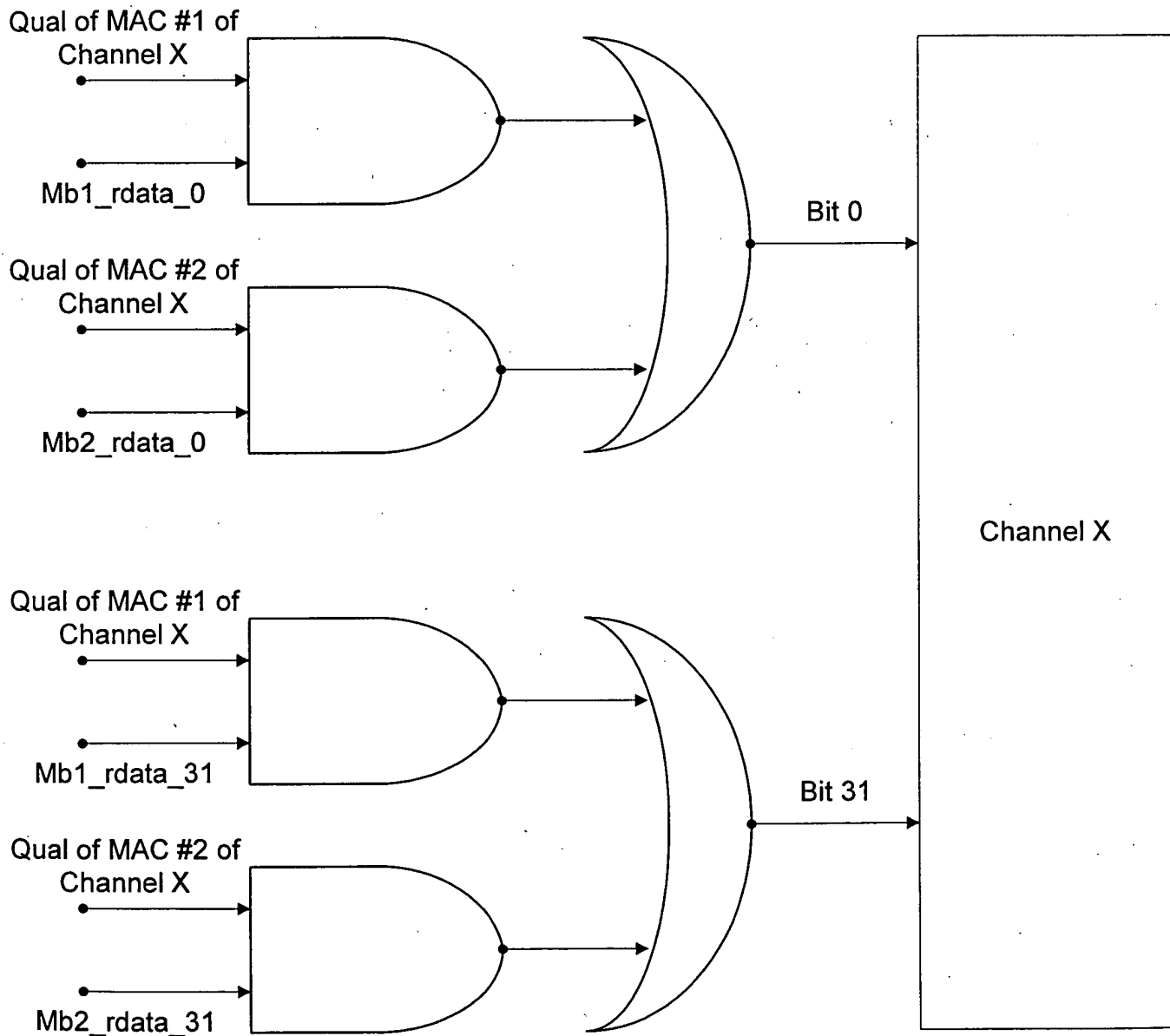


FIG. 14

RE TIME LOAD MANAGEMENT

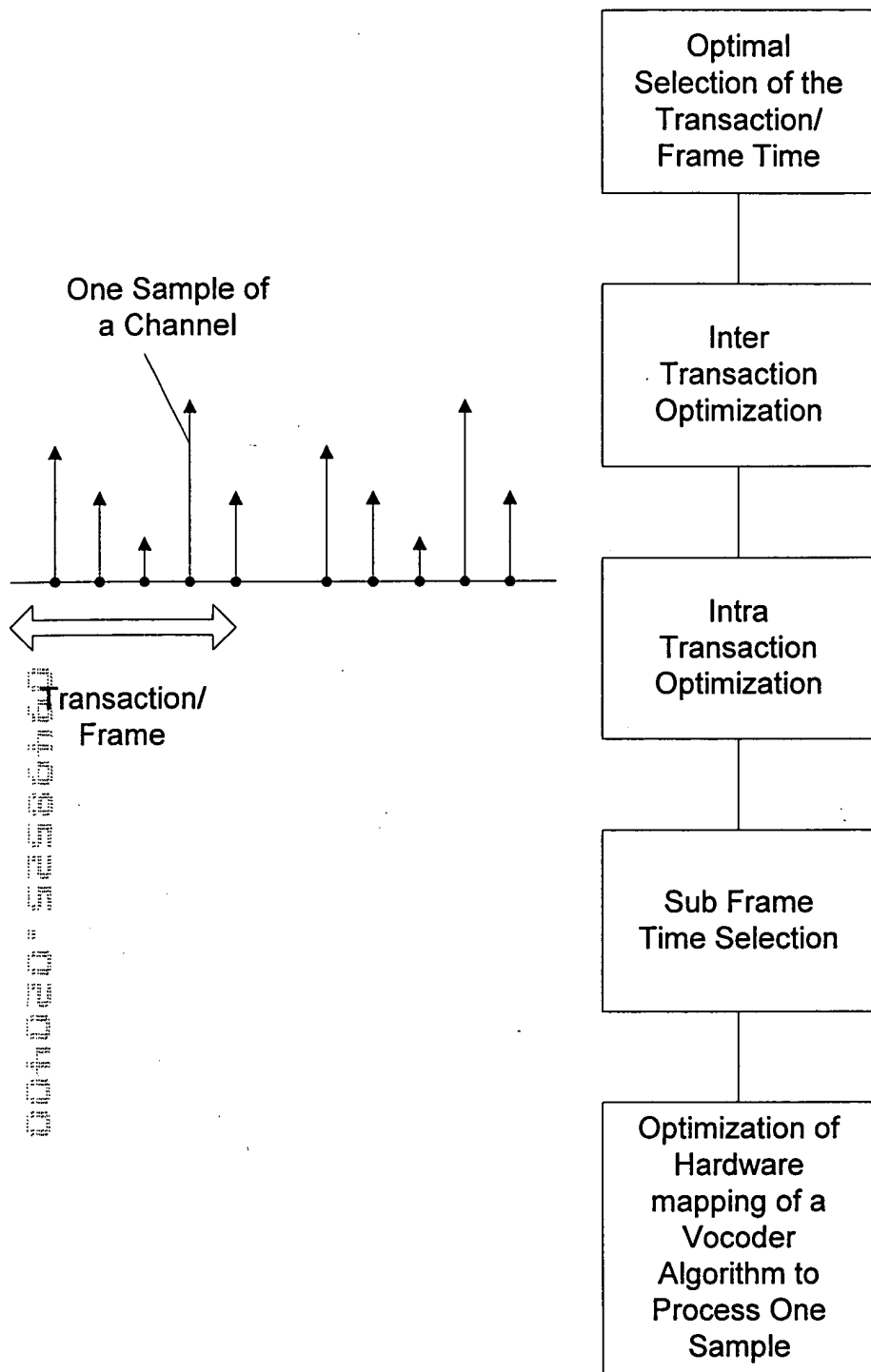


FIG. 15

DLMS PARALLEL WORD TRANSFER

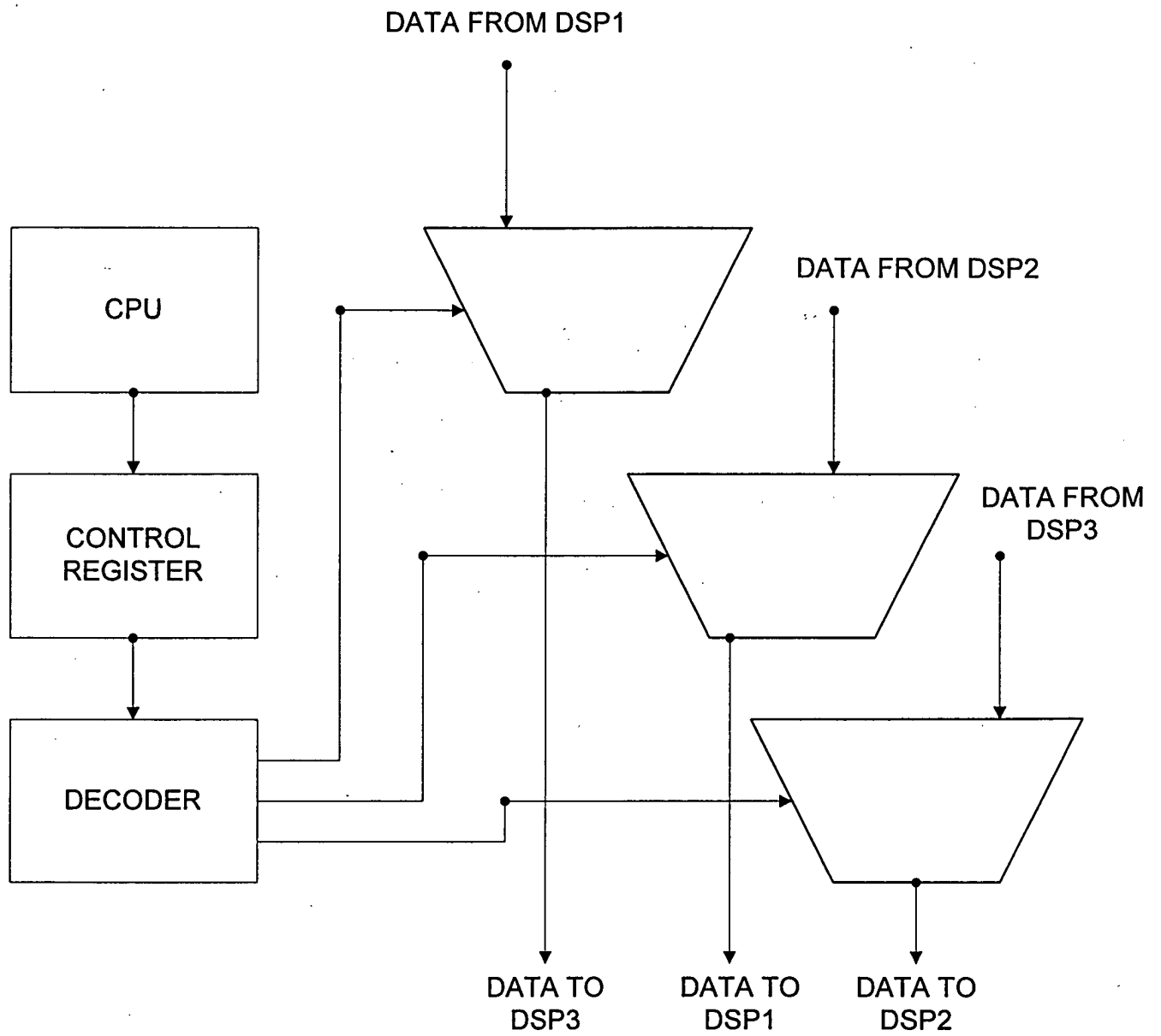


FIG. 16

PE ARRAY

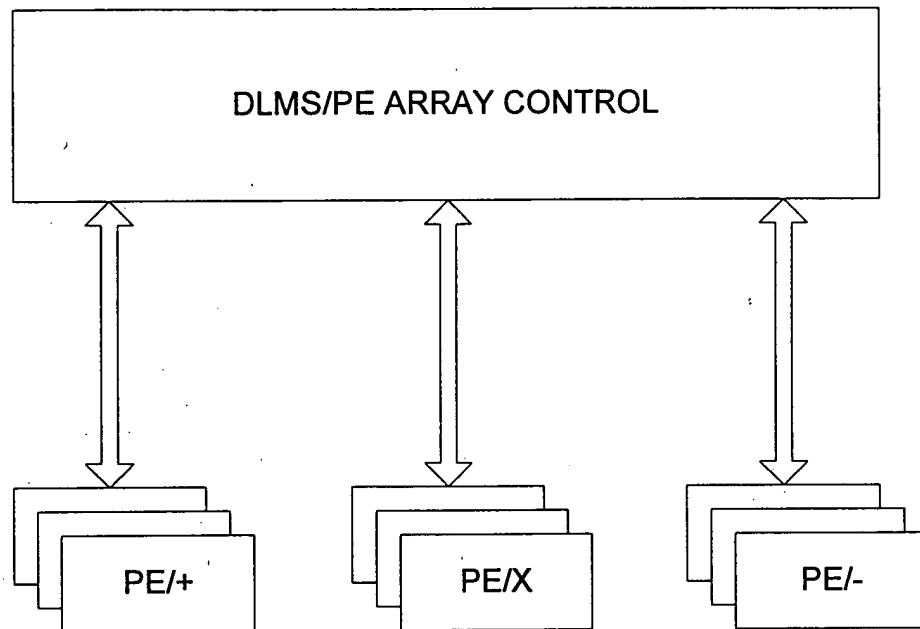


FIG. 17

DocId: 3236160

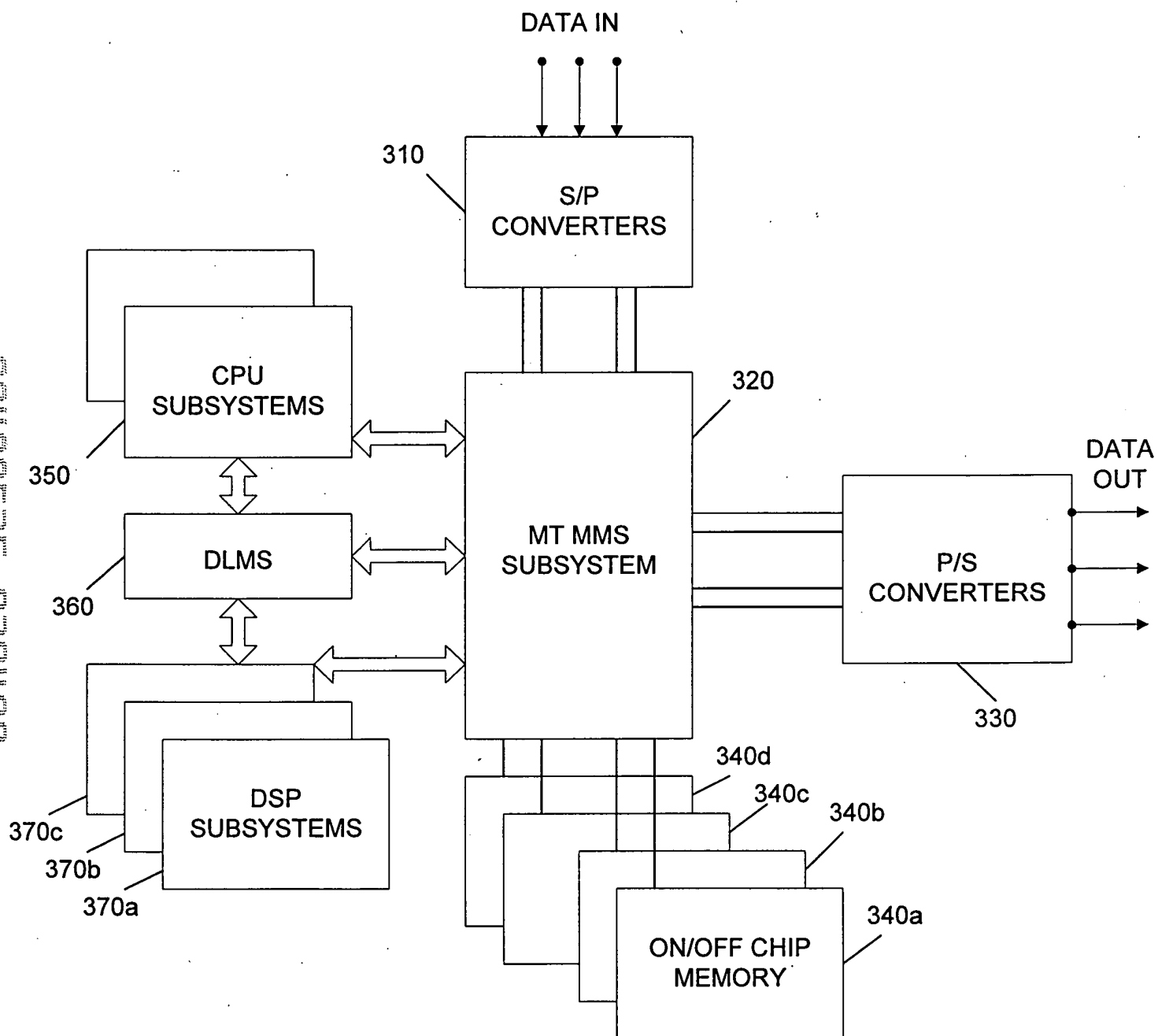


FIG. 18A

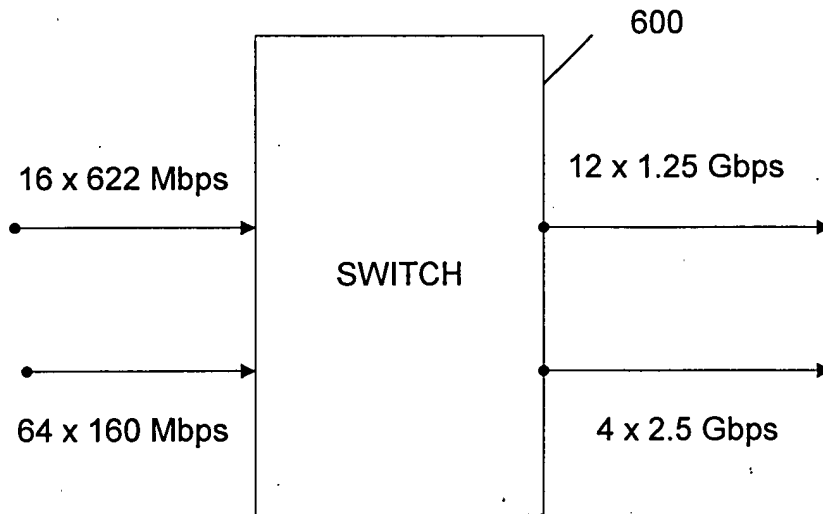


FIG. 18B

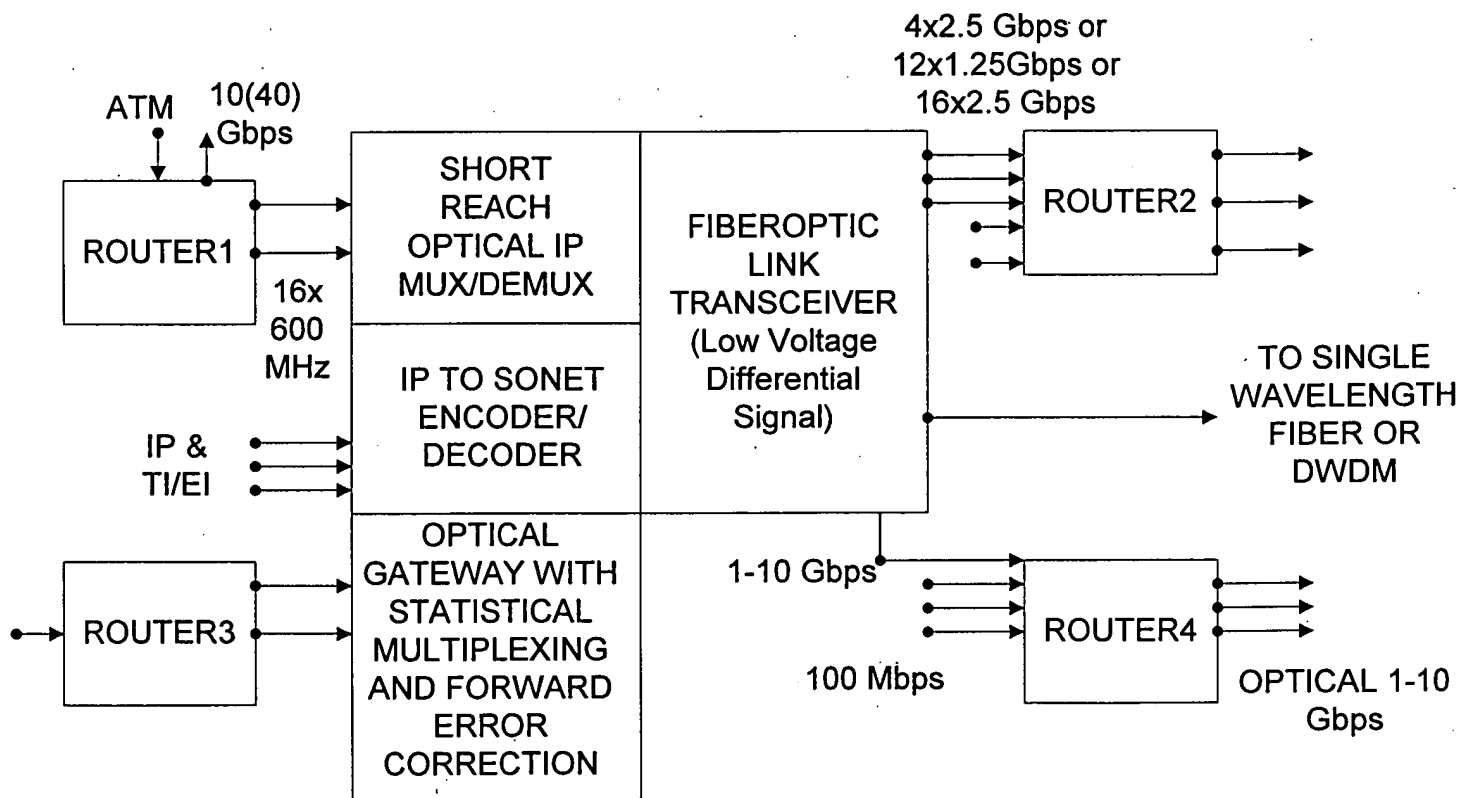


FIG. 18C